# System-Level Analysis

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## Introduction

System-level analysis play an important role in modern electronic system design. For most practical purposes, system-level analysis can be divided into parallel-bus analysis (PBA) and serial-link analysis (SLA) for signal transmissions. This writing is mainly concerned with PBA and SLA for signals. The topic of power distribution networks (PDN) analysis is treated separately.

With very few exceptions all parallel busses and serial links are consisted of transmitters (Tx), receivers (Rx) and the linear passive interconnects between them. One of the main objectives of parallel bus and serial link analysis is to obtain the time-domain waveforms at the receiver (Rx) input in order to determine system performance and design compliance.

## Component Models

The available models for Tx and Rx circuits include HSpice device models (encrypted or unencrypted), IBIS behavioral models, and VHDL/Verilog models.

Models for interconnects are mostly available as SNP network parameters or RLC type models.

## Algorithms and Tools

SPICE is one of the most widely used tools in transient analysis of non-linear systems. Based on the approach to solve time-domain differential equations, it practically is the standard tool of choice in circuit simulation. However when dealing with network parameters, transmission lines, and large device count networks, it often encounters various issues including model availability, longer runtimes, instability and difficulty of user interface, despite various improvements over the years.

ADS offers a transient-convolution engine to solve problems in time-domain based on frequency-domain data. Operational details of the algorithm is largely unpublished and its performance vary.

IBIS and IBIS-AMI behavioral models are based on a prescribed set of external characteristics of the Tx/Rx devices. These models are widely available in the industry. Unlike SPICE models which are based on a set of BCEs and governing laws of KVL and KCL, IBIS models provides circuit responses for a fixed set of voltage, temperature and impedance conditions. It must be “reverse engineered” into a mathematical model usable in transient simulations. This reverse-engineering process carried out by EDA tools is subject to certain degree of uncertainty due to various interpretations of the IBIS Specification.

Network parameter matrices have become the universal choice for representing linear time-invariant (LTI) systems such as signal interconnects or power delivery networks. A number of issues exist when using frequency-domain network parameters in time-domain analysis. Among those are causality, passivity, stability, lack of DC value, etc. Both HSPICE and ADS have experienced long runtimes when simulating network parameters in time-domain.

In the field of signal and power integrity analysis for electronic component and system design, industry practitioners have to cope with a combination of issues involving data incompleteness, tool deficiencies and algorithm uncertainties. Better approaches and tools are needed to solve engineering problems in a robust, clear, efficient manner.

## Behavioral Models

Behavioral models are at the core of parallel bus and serial link analysis. IBIS models are arguably the most widely adopted behavioral models in circuit and system analysis. IBIS-AMI is the extension to IBIS Specification designed for serial link analysis.

IBIS contains a fair amount of legacy contents that are mostly irrelevant to modern high-speed designs. IBIS also has inadequate support on process/voltage/temp (PVT) variations, register/parameter-driven models and automation.

IBIS models have the benefits of not revealing process and circuit information. They are also non-linear models which can be used in transient analysis if processed properly.

IBIS-AMI models are incorporated into the IBIS Specifications for serial link analysis. Due to ambiguities in the specifications and complicated workflows, IBIS-AMI simulations are notoriously known to produce results which are only useful to those “who already know the answer” (quoting a serdes architect who used IBIS-AMI models). IBIS-AMI also suffers from a set of excessively complicated and confusing syntax rules, which could only be interpreted by very few experts on the subject.

## Behavioral Modeling Objectives

Over the years the authors have developed a set of models, algorithms and workflows suitable for parallel bus and serial link analysis. The new models are designed with clarity and rigor, allowing the users to focus on solving the problems at hand, rather than solving the problems of the tools.

Detailed derivations are provided separately. The following is a summary list of the design objective and characteristics of the new modeling approach.

The new approach focuses on the following important areas for innovation and improvement.

1. configurability: effectively manage and support large numbers of configurations and settings such as gain, swing, impedance
2. PVT support: rigorously and unambiguously support all PVT corners
3. Non-linearity: must be inherently non-linear, while at the same time capable of working with LTI engines by domain-decomposition
4. DC/AC: must adequately support both DC and AC analysis
5. Power accurate: rather than simply being power-aware, these models are true and accurate in power
6. Rigorous: rigorous models rely on proven electrical and physical laws to get the correct answers, they do not rely on ambiguous interpretations and unpredictable interventions to get the correct results
7. Uniqueness: produces unique results at a given set of parameters
8. Flexibility: the models should have little or none arbitrary restrictions on their behaviors, they simply adhere to universal laws of engineering

## Serial Link Analysis

At present, IBIS-AMI is the industry standard for high-speed serial link modeling. The basic approach of the algorithmic modeling interface (AMI) is to encapsulate the Tx and Rx functions into a pair of signal processing blackboxes with associated analog whiteboxes which are passive and linear time invariant. The mathematical derivations of IBIS-AMI modeling have been completed by the authors through several revisions and a matlab prototype have been coded.

One of the main obstacles in IBIS-AMI modeling is to navigate a myriad of ambiguous and implicit definitions in the specifications in order to obtain and interpret the necessary information. After years of research and investigation, this obstacle has largely been lifted.

In addition, a new approach has been derived to cope with issues related to impulse response derivation, multiple reflection and non-ideal terminations.

The tasks on hand include the following:

1. Implement the algorithms in C++
2. Develop test cases to compare results between commercial software and own algorithms
3. Compare results between convolution, ifft and vector fitting methods
4. Derivations on obtaining impulse response through Fourier and Laplace transformations,
5. Investigate some programmatic pros and cons of IBIS-AMI models, recommend improvements
6. To define, implement and test the new format for serial link behavioral models
7. Implement crosstalk analysis in SLA

## Parallel Bus Analysis

The challenges in PBA are somewhat different from those of SLA in the following aspects:

1. Large number of pin counts and associated logistics to setup the problem
2. IBIS models having a different set of parameters and methods from IBIS-AMI
3. Non-linearity and time-variance of driver output impedance
4. Diverse and complex schemes of compliance
5. Extraction of large pin-count interconnects
6. Availability and Idiosyncrasies of existing tools
7. Lack of jitter and timing budgets of driving signals and entire system
8. Largely inadequate and inappropriate support for SSN/SSO analysis
9. accuracy of IBIS models

The PBA project could make contributions in following areas:

1. verify and improve accuracy of IBIS models
2. automation of large number of simulations and reporting
3. design rule setup, verification and management
4. capture and verify compliance schemes
5. assessment of design margins

References

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[2] IBIS Specification 5.0, 5.1

[3] Technical Staff, Texas Instruments Incorported, Application Report, SLLA067B–March 2000–Revised October 2009, Comparing Bus Solutions